UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,236,057 B2
APPLICATION NO. : 10/647929
DATED : June 26, 2007
INVENTOR(S) : Masao Kaizuka

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

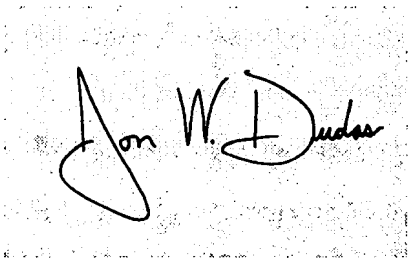
Delete the title page and substitute therefore the attached title page.

Delete Drawing Sheets 1 of 3 and 2 of 3 and substitute therefore the attached Drawing Sheets 1 of 3 and 2 of 3.

Column 13, line 24, replace "signal and A is" with --signal and Δ is--.

Signed and Sealed this

Thirteenth Day of November, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Kaizuka

(10) **Patent No.: US 7,236,057 B2**
(45) **Date of Patent: *Jun. 26, 2007**

(54) **SPREAD SPECTRUM CLOCK GENERATOR**

(75) Inventor: Masao Kaizuka, San Jose, CA (US)

(73) Assignee: Toshiba America Electronic Components, Inc., Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 630 days.

This patent is subject to a terminal disclaimer.

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(22) Filed: Aug. 26, 2003

(65) **Prior Publication Data**

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(51) **Int. Cl.**
H03L 7/00 (2006.01)

(52) **U.S. Cl.** ..... 331/1 A; 331/78; 332/123; 375/130; 375/376; 713/500

(58) **Field of Classification Search** ..... 375/376, 375/130; 327/156; 332/123; 713/500; 331/1 A, 331/78

See application file for complete search history.

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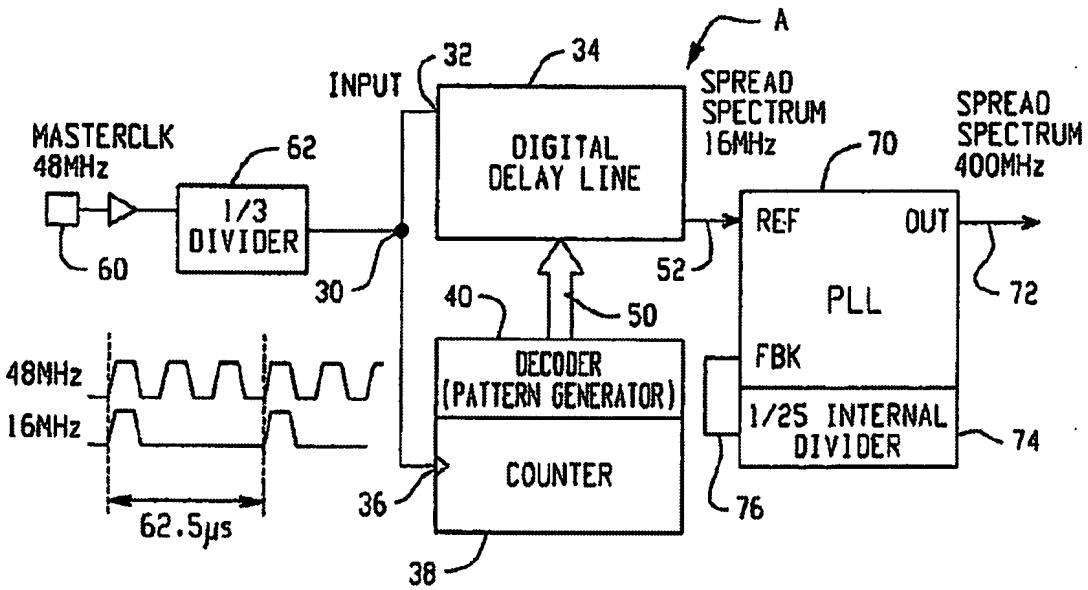
(57) **ABSTRACT**

A clock signal generator varies a frequency of a digital clock over a selected range of frequencies. The generator employs a divider for lowering a frequency of a clock signal. A counter increments synchronously with the signal, and causes a selected sequence of outputs to be generated by a pattern generator. The pattern generator output forms an input to a digitally controllable delay line which receives the lower frequency clock signal. The pattern generator causes the digital delay line to vary a frequency of the lowered frequency clock signal between selected boundaries. The varying frequency clock signal is then raised up again such that a final clock has a varying frequency, and will exhibit less EMI spiking during switching of an associated, synchronous digital data device. The solid state nature of the generator allows for simple fabrication, inexpensive manufacture and ready integration into digital circuitry, such as multifunction integrated circuits.

15 Claims, 3 Drawing Sheets



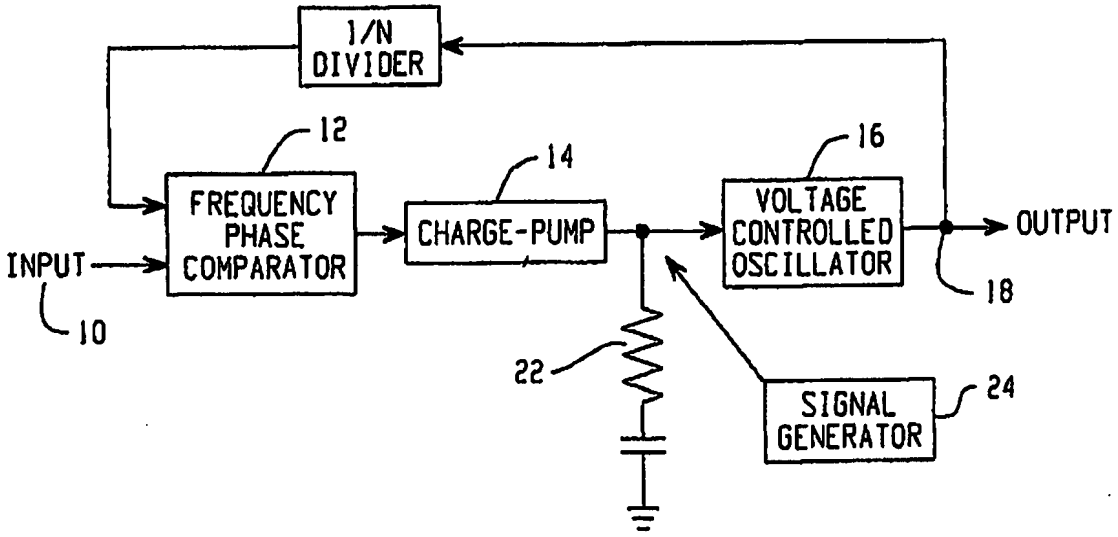


Fig. 1A
PRIOR ART

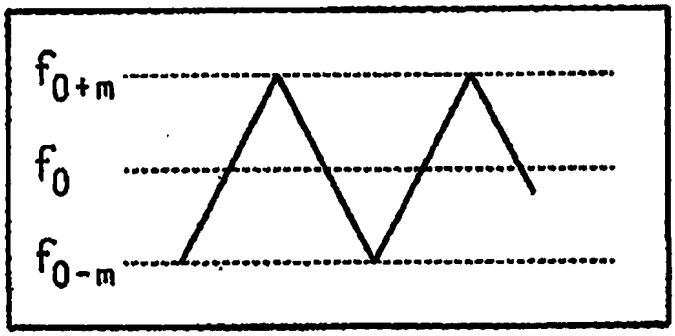


Fig. 1B

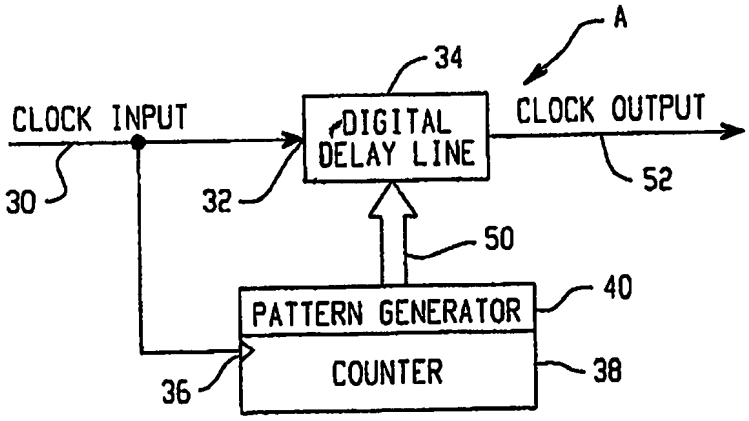

A
34
CLOCK INPUT
DIGITAL DELAY LINE
CLOCK OUTPUT
30
32
52
50
PATTERN GENERATOR
40
COUNTER
36
38

Fig. 2

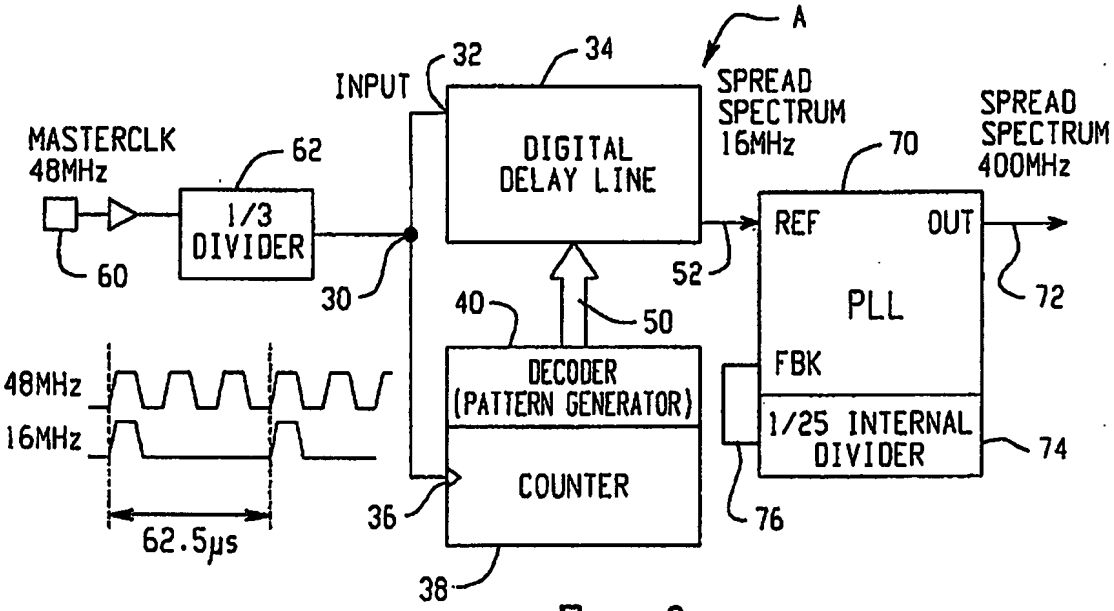

A
INPUT
32
34
SPREAD SPECTRUM 16MHz
SPREAD SPECTRUM 400MHz
MASTERCLK 48MHz
62
70
DIGITAL DELAY LINE
1/3 DIVIDER
REF
OUT
60
30
52
72
PLL
40
50
FBK
48MHz
DECODER (PATTERN GENERATOR)
1/25 INTERNAL DIVIDER
74
16MHz
COUNTER
36
76
62.5μs
38

Fig. 3